

Page 20, between lines 11 and 12, insert the following centered heading and succeeding

paragraphs:

B2

BRIEF DESCRIPTION OF THE DRAWINGS

Figures 1 (a) through (d) show cross-sectional views of the steps in the TFT fabrication process of the present invention.

Figure 2(a) is a schematic diagram showing the essential components of the RTA unit used for the second annealing step in the present invention.

Figure 2(b) explains the annealing state during the second annealing step.

Figure 2(c) shows the temperature profile in the RTA unit.

Figure 3 shows the relationship between the annealing temperature, the annealing time, and the resulting effect (TFT mobility) for the second annealing step in the present invention.

Figure 4 shows the relationship between the time factor β during the second annealing step in the present invention and the effect (TFT mobility) of the second annealing step.

Figure 5 shows the relationship between the time factor β and the resulting effect (variation in TFT mobility) for the second annealing step in the present invention.

Figures 6 (a) through (d) schematically show in cross-section the process steps of one portion of the fabrication procedure for solar cells according to the present invention.

Figures 7 (a) through (d) schematically show in cross-section the process steps of one portion of the fabrication procedure for solar cells according to the present invention.

Figures 8 (a) through (d) schematically show in cross-section the process steps of one portion of the fabrication procedure for solar cells according to the present invention.

Figures 9 (a) through (c) are schematic diagrams of the essential components of the annealing unit used in the first annealing step of the present invention.

Figures 10 (a) through (d) schematically show in cross-section the process steps of one portion of the fabrication procedure for solar cells according to the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Page 49, line 14 to page 50, line 10, delete in its entirety.

Page 50, between lines 18 and 19, insert the following centered heading:

EXAMPLES

Page 66, line 35 to page 67, line 26:

Then a tantalum (Ta) thin film, which becomes gate electrode 15, is deposited by means of sputtering. The substrate temperature at the time of sputtering is 150°C, and the film thickness is 500 nm. Patterning is carried out after the tantalum thin film, which is to become the gate electrode, is deposited. This is followed by implantation of impurity ions in the semiconductor layer and formation of source and drain regions 16 and channel region 17 (FIG. 1(c)). In this example, because CMOS TFTs are being formed, NMOS TFTs and PMOS TFTs are formed on a single substrate. The PMOS TFTs are covered with polyimide during formation of the sources and drains of the NMOS TFTs; conversely, the NMOS TFTs are covered with polyimide during formation of the sources and drains of the PMOS TFTs, thereby making CMOS TFTs. At this time, the gate electrode serves as a mask for ion implantation, and the channel becomes a self-aligned structure that is formed only below the gate electrode. Impurity ion implantation is carried out using a non-mass separating ion implanter and phosphine (PH₃) or diborane (B₂H₆) diluted by hydrogen to a concentration of approximately 5% as the source gas. For NMOS, the total ion implantation dose, including ions such as PH₃⁺ and H₂⁺, is 1 x 10¹⁶ cm⁻² and the phosphorous atom concentration in the source and drain regions is approximately 3 x 10²⁰ cm⁻³. Similarly, for PMOS, the total ion implantation dose, including ions such as B₂H₆⁺ and H₂⁺, is also 1 x 10¹⁶ cm⁻² and the boron

atom concentration in the source and drain regions is approximately $3 \times 10^{20} \text{ cm}^{-3}$. The substrate temperature at the time of ion implantation is 250°C.

Page 67, line 27 to page 68, line 3:

Next, interlevel insulator layer 18, comprised of a silicon oxide film, is formed by means of PECVD using TEOS. The substrate surface temperature during interlevel insulator layer deposition is 350°C., and the layer thickness is 500 nm. After the interlevel insulator layer is formed, thermal annealing is performed for 1 hour at 350°C. in an oxygen atmosphere to achieve activation of implanted ions and densification of the interlevel insulator layer. Contact holes are then opened to the source and drain regions, and aluminum (Al) is deposited by means of sputtering. The substrate temperature during sputtering is 150°C., and the film thickness is 500 nm. Patterning is carried out on the aluminum thin film source and drain electrodes 10 and interconnects to complete the thin film semiconductor device (FIG. 1(d)).

Page 68, lines 4-11:

In this example, with the goal of investigating the transistor performance and the nonuniformity within a single substrate, 50 transistors uniformly fabricated over a large substrate and having channel lengths $L=5 \mu\text{m}$ and widths $W=5 \mu\text{m}$ were measured. The results are as shown below. The on current is defined at $|V_{ds}|=4 \text{ V}$ and $|V_{gs}|=10 \text{ V}$ while the off current is defined at $|V_{ds}|=4 \text{ V}$ and $|V_{gs}|=0 \text{ V}$.

Page 71, line 4, delete in its entirety.